

### PCM Communications Demodulator FOR TELECOMMUNICATIONS SIGNALS RECEPTION

#### Key Features

- **Satellite and Terrestrial Communications Link Reception**
- **Special Fine Tuning Controls for use with severely degraded transmissions**
- **Multiple IF selections**
- **PSK, QAM, MSK, and FSK demodulation**
- **Wide Band Rates**
- **Various FEC formats supported Convolutional and Block codes with De-Interleaving**
- **32 Tap Self Synchronous and Additive PRN/LRS decoding supported**
- **4 levels of Demultiplexing Programmable for Standard and Non-Standard formats**
- **Configuration stored for library recall of signals of interest**
- **VGC audio output monitor**
- **Built in translation for Pre-D record and playback**
- **Removable Flash Drive**
- **Remote Control via LAN**

TriaSys Technologies' 7500TR PCM Demodulator, in conjunction with any phase stable receiver, provides the capability for real time demodulation and analysis of Standard or Non-Standard PCM transmissions.

The 7500TR is designed for use with transmissions that have been severely degraded from low carrier-to-noise signal levels and adjacent spurious interference carriers. Adjacent channel interference is minimized through the use of Surface Acoustic Wave (SAW) Intermediate Frequency (IF) band pass filters. The SAW IF filters result in excellent out-of-band rejection while maintaining flat in-band envelope delay (phase) characteristics. The Adaptive Blind Equalizer provides further noise rejection. The Implementation of Controls to fine tune this performance allows the 7500TR to out perform standard modems.

With 4 levels of Special Format PCM processing few signals can escape the 7500TR's grasp. The programmable PRN descrambler for Self Synchronous and Additive PRN/LRS formats is also available at all levels.



The 7500TR runs on the Windows® 2000 Professional operating system, with a user friendly GUI.

The 7500TR can decode A-Law, Mu-Law, ADPCM, CVSD and Sign Magnitude encoded Voice Grade Channel (VGC). The unit provides for monitoring channel activity on a display.

General self testing is provided through built-in-test-equipment (BITE).

The 7500TR can be integrated with TriaSys' Signal Collection Servers (SCS) or TriaSys' the Voice Channel Monitor, VCM7500, and combined with other TriaSys software products, to provide a complete "signal-to-analyst" solution.

With the addition of an SCS from TriaSys additional capabilities can be realized such as, SS7 analysis and monitoring, Call Recording, decode GSM Audio formats and much more.

### TRIASYS

### TECHNOLOGIES

### CORPORATION

## Model 7500TR Performance Specifications

#### Carrier Inputs

- IF Receiver Carrier: Six selectable IF Carriers to support HF, VHF, UHF and SHF receivers: 455 kHz, 10.7 MHz, 21.4 MHz, 70 MHz, 140 MHz and 160 MHz.

#### IF Carrier Input Levels

- IF Receiver Inputs: Automatic Gain Control (AGC) automatically controls receiver output levels from -55 dBm to 0 dBm.

#### Pre-Detection Record/ Playback

- Programmable to record and playback any carrier frequency in the range from 455 KHz to 20 MHz from analog or digital pre-detection recorders.

#### IF Carrier Bandwidths

- Automatic programming algorithms select the correct IF SAW filters for the processing of the signal of interest based on the signal's symbol rate.

#### Baseband Data Inputs

- Input ports are provided to accept baseband signals: analog 1Vpp max; NRZ-L/M/S data with levels from 0.15 to 2.5 Vpp.

#### Bit Synchronization

- Programmable, within 1 bit/sec, for symbol rates of 64 K s/s to 25 M s/s symbol clock recovery Maxim Rate 50 Mbits/s. Max and min rates vary with modulation, consult factory for a specific requirement.

#### Bit Decoding

- Programmable bit decoding algorithms are provided for NRZ-L, NRZ-M, and NRZ-S.

#### Demodulation Modes

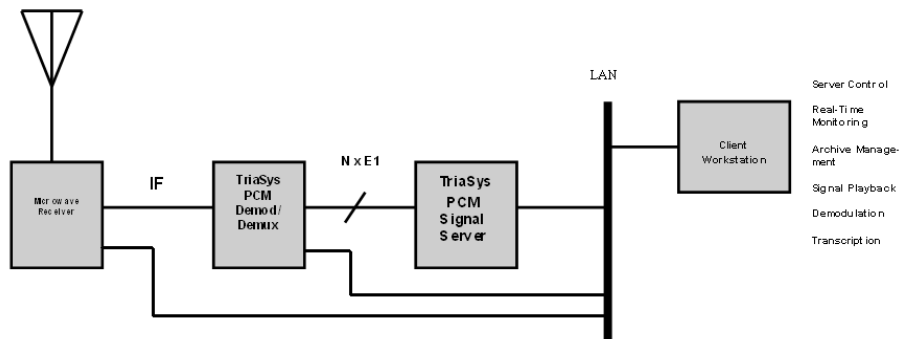
- BPSK; QPSK; DQPSK; SQPSK/OQPSK; PI/4 DQPSK; 8 and 16 PSK; 16, 32, and 64 QAM (absolute and differential) MSK; 2, 4, and 8 FSK.

#### Symbol to Bit Mapping

- Automatic sector to bit mapping algorithms are provided for BPSK, QPSK, OQPSK, 2 Level FSK, and MSK for both absolute and differential encoding. Programmable symbol to bit mapping GUIs, absolute and differential, provided for: QPSK, 4 & 8 FSK, 8 & 16 PSK, 16, 32 & 64 QAM.

#### FEC Decoding

- Convolutional Codes: Viterbi decoding, constraint length 7, is provided for Rates 1/2, 1/3, 2/3, 3/4 and 7/8. Trellis decoding is provided for 8 PSK Rate 2/3 and 16 PSK Rate 3/4 (PTCM).
- Block De-Interleaving: Fixed selection and programmable for any N (message length), K (block length = N + check bits), and L (Interleaving depth including standard 2, 4 and 8).
- R-S Decoding: Selectable menu programming for Reed-Solomon Forward Error Correction (FEC) decoding.



PCM Processing Example

## Model 7500TR Performance Specifications continued

### PCM TDM De-multiplexing

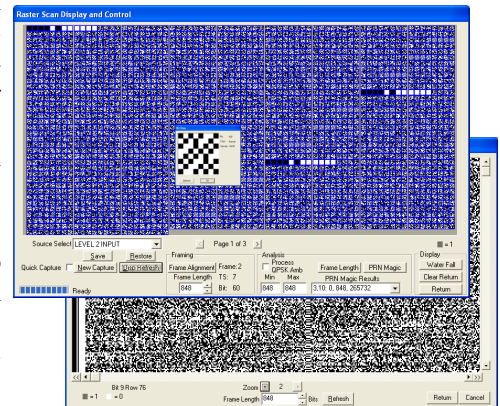
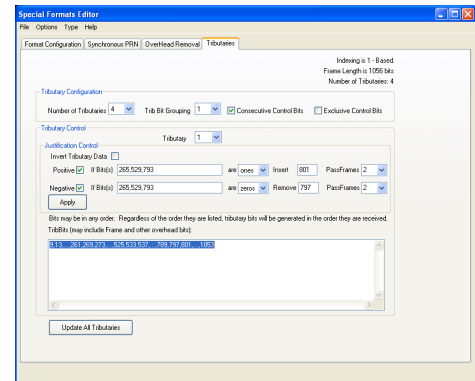
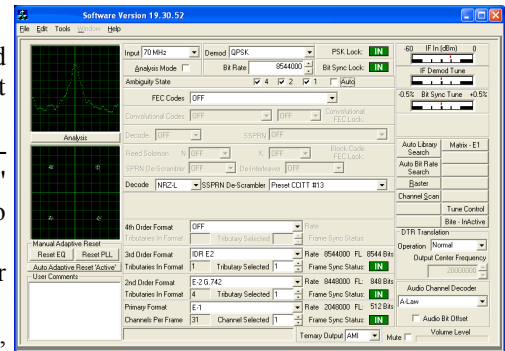
- **Stored Programming:** Pre Stored configurations for quick recall provided for: G.732 E1 2.048 Mb, G.742 E2 8.448 Mb, G.751 E3 34 Mb and Intelsat IDR formats.
- **Manual Programming:** Standard, or non-standard, PCM format can be programmed for de-multiplexing through the user friendly "Special Formats" GUI. These special formats can be stored to a library for quick recall to allow for:
  1. Overhead bit removal of justification bits, framing bits, and any other stuffed bits for bit and byte interleaved TDM formats
  2. Frame Alignment Synchronization (FAS) patterns greater than 128 bits, bits can be consecutively ordered or dispersed among frame
  3. Higher order format programming supports super frame lengths of up to 130,000 bits
  4. De-multiplexing for level 1, 2, 3, and 4 TDM formats or bit manipulation such as Block Interleaving, available for L2, L3, and L4
  5. Programmable positive and negative justification for up to 16 control bits over 16 consecutive frames for L2, L3, and L4
  6. Additive / Synchronous PRN/LRS decoding at all levels
  7. Self synchronous PRN/LRS decoding at all levels
  8. NRZ-M, -S and Data Invert programmable at all levels
  9. Programmable frame lock algorithm at all levels

### Synchronous PRN

- **Manual Set Up Mode:** At the decode level programmable up to 32 tap length and up to 6 rails and at every other level programmable up to 32 tap length and up to 31 rails for Maximum Length Sequences (MLS) and non MLS sequences both normal taps or inverted taps. Other formats also supported i.e. Intelsat IESS309 Decoding, V.35. PRN decoding can be programmed for use on level 1, 2, 3 and 4 PCM signals along with the decoder level processing.
- **PRN search:** Search algorithm to analyze and determine PRN based on commonly used formats.

### Additive PRN

- **Manual Setup Mode:** Programmable setup to library storage for recall, to support additive PRN encoding based on framing synchronization pattern used, preset patterns and encoding frame length.
- **Search Mode:** scanning search algorithm to locate unknown Assigned Synchronization Markers (ASM/ Frame Sync) and the frame length.



## Model 7500TR Performance Specifications continued

### *Signal Analysis*

- Analysis algorithms and displays include:
  1. Automated detection of an unknown symbol rate, bit rate, frame length, and PRN encoding
  2. Detection of self synchronous PRN and ASM for additive PRN
  3. Save and Recall Digital snapshot for further analysis (up to 16 megabits)
  4. Waterfall display for analysis of overhead bits, framing patterns, and frame lengths
  5. VGC Scan display (4 or 8 bit selectable)
  6. Spectrum and constellation displays (vector display to distinguish QPSK / OQPSK)
  7. Library search mode for received signals, optionally based on bit rate

### *System Configuration*

- Unlimited Save and Recall of all user parameters that are part of the system configuration with built in Database search for SOI.

### *Voice Grade Channel Decode*

- VGC decoding programmable for 8-bit A-LAW, Mu-LAW and Sign Magnitude, 2, 3, 4 and 5-bit ADPCM both A-LAW and Mu-LAW, 1 through 8-bit CVSD both military and telecom. VGC selection as either individual channel or position bit.

### *Output Data Ports*

- Ports are provided for analysis and down stream processing for:
  1. I/Q blind equalized outputs, serial data and clock
  2. A single primary (E1) Ternary HDB3 output from a Level 1 input signal
  3. Four simultaneous primary Ternary outputs from a Level 2 (E2) input signal
  4. Matrix selection, select any eight E1 tributaries from a standard E3 G.751 to output as HDB3
  5. Sixteen simultaneous E1 Ternary HDB3 outputs from a standard E3 G.751 input signal

### *Built In Test*

- Built-In Test Equipment (BITE) provides a general functionality test capability.

## **To Inquire or Order**

For a demonstration, further information, or to contact a representative, please call 978.244.1060, or visit our website at [www.triasys.us](http://www.triasys.us).

### *Processing Unit*

- The CPU is an Intel Pentium based Processor performance and support parameters are:
  1. Windows® 2000 Professional operating system
  2. Two USB ports on front panel and a single USB port on rear panel
  3. Secured Removable Flash drive
  4. Ethernet Interface on rear panel

### *Remote Control*

- LAN remote control provided via "Remote Admin" (or other remote control software).

### *MTTR*

- MTTR is 30 to 60 minutes, nominal, for repair at the module level.

### *Environmental*

- Storage Temperature: 0 to 50 degrees C, Humidity to 95% without condensation

### *Mechanical and Power*

- 5U rack-mountable chassis (Slides optional)
- 60 pounds nominal weight.
- Front panel color is Federal Std 26492 Gray.
- 110-220 VAC, 48 to 68 Hz with universal power

### *Training*

- Training is available for user and advanced user

Product Formerly a Signami / Signami DCS Product  
The 7500TR is a direct replacement for the Signami 7500EXL

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